

Computer Engineering 315L  
Digital System Design Lab  
Lab3  
Verilog HDL Simulation  
And Sequential Design

**Purpose**

Design and build a Mealy sequence detector finite state machine (FSM). Write Verilog process description for the FSM.

**Assignment**

Design a synchronous sequential circuit with one input  $x$  and an output  $z$ . The input is a serial message and the system reads  $x$  one bit at a time. The output  $z = 1$  whenever the pattern 101 is encountered in the serial message. For example:

If input:       0 0 1 0 1 0 1 1 1 0 1 0 0 0 1 0 1  
Then output:  0 0 0 0 1 0 1 0 0 0 1 0 0 0 0 0 1

Use  $D$  flip-flops with *active-low preset* and *active-low clear* inputs.

Derive the state diagram and the state table. At this point, you should compile and simulate a Verilog process description to verify the correctness of your design. Refer to the Verilog supplement (found on lab webpage) and Mano and Kime page 272-277 for more detail on process description for state diagrams.

Once you had verified the correctness of your state diagram, obtain the simplified equations for the flip-flops inputs and the outputs using K-maps. Build and test your circuit using the prototyping board and ICs.

**Lab Report (checklist and grading)**

- Lab reports should be in a narrative form and should be **typed and well organized**.
- **No** hand-written documentation or hand-drawn schematics or diagrams will be accepted.
- Upon completion of the lab, your lab report should include the following:
  - A cover page with your Name, Lab number and title, CPEN315, Spring 2008, and Date, all in order and in the center of the cover page. **(5 points)**
  - A clear presentation of all steps of your circuit design work, which includes state diagram, K-maps, equations, and circuit diagram. **(40 points)**
  - Verilog HDL code for process description and timing (waveforms) diagram. **(15 points)**
  - You need to demonstrate the correctness of you circuit to the instructor. **(40 points)**