

Computer Engineering 315L
Digital System Design Lab
Spring 2008
Lab4
Registers and Counters

Purpose

The main goal of this lab is to present sequential blocks, generally referred to as registers and counters. The circuits considered here have structured pattern, with multiple stages or cells. Because of this structure, it's easy to add more stages to produce larger systems. Registers are especially useful for storing information during processing of data and counters assist in sequencing the processing.

Assignment

Part I

- a. Write and compile a behavioral Verilog HDL description for a *D positive-edge-triggered* flip-flop with clock CLK. Compile and simulate your description to *demonstrate correctness*.
- b. Write and compile a behavioral Verilog HDL description for a 4-bit register with Parallel Load as shown in Figure 1. Your HDL code will have a D, CLK and LOAD as inputs and Q as output. Compile and simulate your description to *demonstrate correctness*. Refer to Figure 2 as a guide for simulation results.
- c. Extend the 4 bit to a 16-bit register and repeat part b.
- d. After you had explained the operation of the 4-bit binary counter shown in Figure 3, write a Verilog HDL description for the counter using a register for the D flip-flops and Boolean equations for the logic. Compile and simulate your description to *demonstrate correctness*.

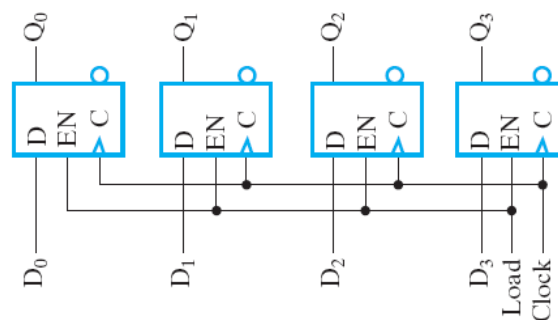


Figure 1. 4-bit register with parallel load

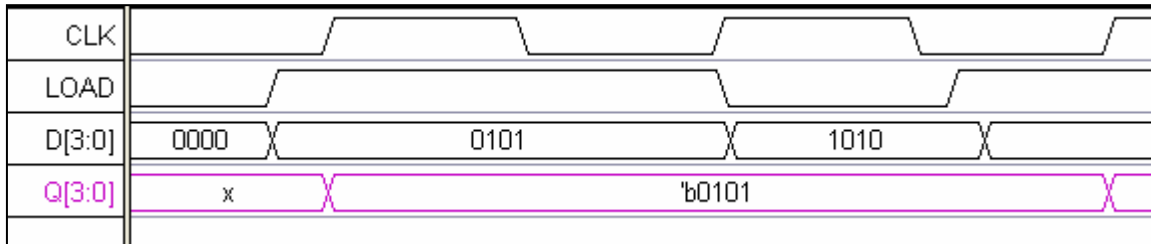


Figure 2. Simulation results of the 4-bit register of Fig.1.

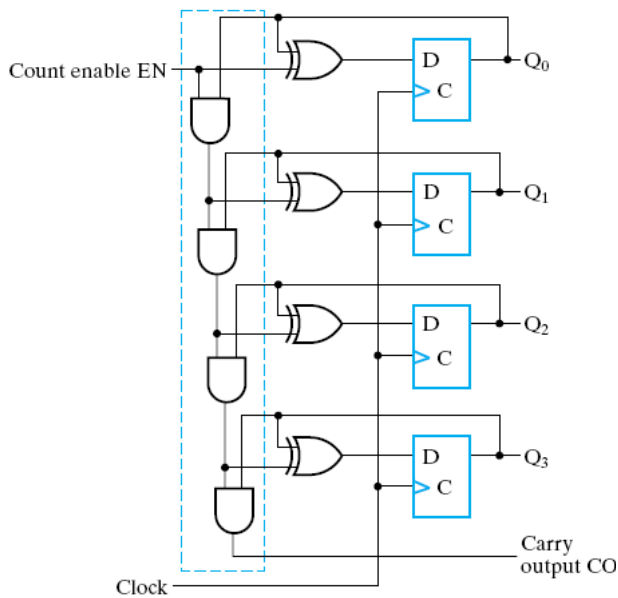


Figure 3. Binary counter

Part II

Design a 2-bit register to be operated according to the following function table. Show the circuit schematics and label all inputs and outputs.

S_1	S_0	Register Operation
0	0	No change
0	1	Clear the register to 0
1	0	Complement output
1	1	Load parallel data

Build and test your circuit using the prototyping board and ICs.

Word of advice: Don't wait till the night before the due date to start working on this lab.

Lab Report (checklist and grading)

- Lab reports should be in a narrative form and should be **typed and well organized.**
- **No** hand-written documentation or hand-drawn schematics or diagrams will be accepted.
- Upon completion of the lab, your lab report should include the following:

Part I

- A cover page with your Name, Lab number and title, CPEN315, Spring 2007, and Date, all in order and in the center of the cover page. **(5 points)**
- Circuit diagrams for part I. **(5 points)**
- Verilog HDL code and timing diagrams for part I. Verifying correctness. **(45 points)**
- Explanation of the counter operation. **(5 points)**

Part II

- Circuit diagram. **(10 points)**
- You need to demonstrate the correctness of you circuit to the instructor. **(30 points)**