

```
module mealy (clk, x, z);

input clk, x;
output z;
reg [2:0] state;

parameter [2:0] zero = 2'b00, one = 2'b01, two = 2'b10;

assign z = x & state [1];

always @ (posedge clk)
  case (state)
    zero: if (x ==0)
      state <= zero;
    else
      state <= one;
  .
  .
  .
```

