

HARDWARE LAB 3
Designing Digital Counter Using Flip-Flops

NAME _____ SECTION _____

A digital counter is a device that generates binary numbers in a specified count sequence. The counter progresses through the specified sequence of numbers when triggered by an incoming clock waveform, and it advances from one number to the next only during the occurrence of a clock pulse. The counter cycles through the same sequence of numbers continuously so long as there is an incoming clock pulse.

You are to build a 3-bit synchronous count-down counter, which is a counter that counts down goes through the binary states 111 to 000 and back to 111 to repeat the count. You are to use IC type 74LS76 (dual positive-edge-triggered *JK* flip-flops). The pin assignment diagram for 74LS76 is shown in Fig. 11-12 on the second page. Construct a state machine excitation table with the following headings:

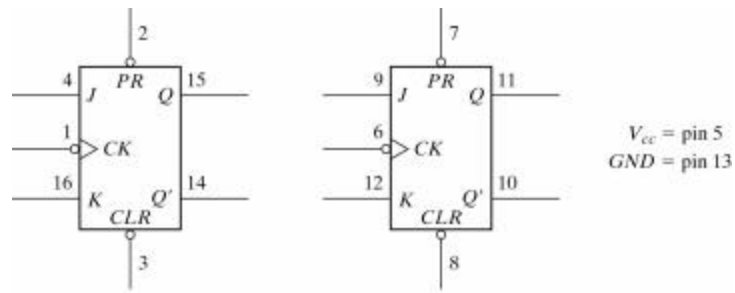
Present State Next State Flip-flop inputs (1 column for each flip-flop input)

The present state portion will have a column for each bit needed in the counter design and should enumerate the count sequence. The next state columns should enumerate which state the counter should go to next, given the present state. For example, if circuit is in a present state of 1 the next state in a down-count sequence would be 0.

1. Once you had completed the excitation table, use K-maps to derive the Boolean expression for each of the flip-flop's input as a function of the present state.
2. Draw the schematic diagram of your circuit. Clearly label the MSB and the LSB on the diagram.
3. Connect the IC-type 555 timer unit shown in Fig. 11-21 and use it to produce clock pulse that will trigger the flip-flops in the counter circuit. Use $R_A = 0.5\text{ M}\Omega$, $R_B = 20\text{ M}\Omega$, and $C = 0.047\text{ }\mu\text{F}$. The 10-M Ω resistor is coded with brown, black, and blue stripes and the 0.5-M Ω resistor is coded with green, blue, and yellow stripes. This RC configuration should produce a clock frequency close to 1.0 Hz.
4. Couple the output of the clock pulse generator to the clock in your synchronous counter circuit.
5. Verify that the counter goes through the count sequence.

The grading for this lab is as follows:
(30% report and 70% demo)

This handout with name..... 1%
State machine excitation table.... 12%
K-Maps and equations..... 12%
Circuit diagram..... 5%



Function table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1		0	0	No change	
1	1		0	1	0	1
1	1		1	0	1	0
1	1		1	1	Toggle	

Fig. 11-12 IC Type 7476 Dual JK Master-Slave Flip-Flops

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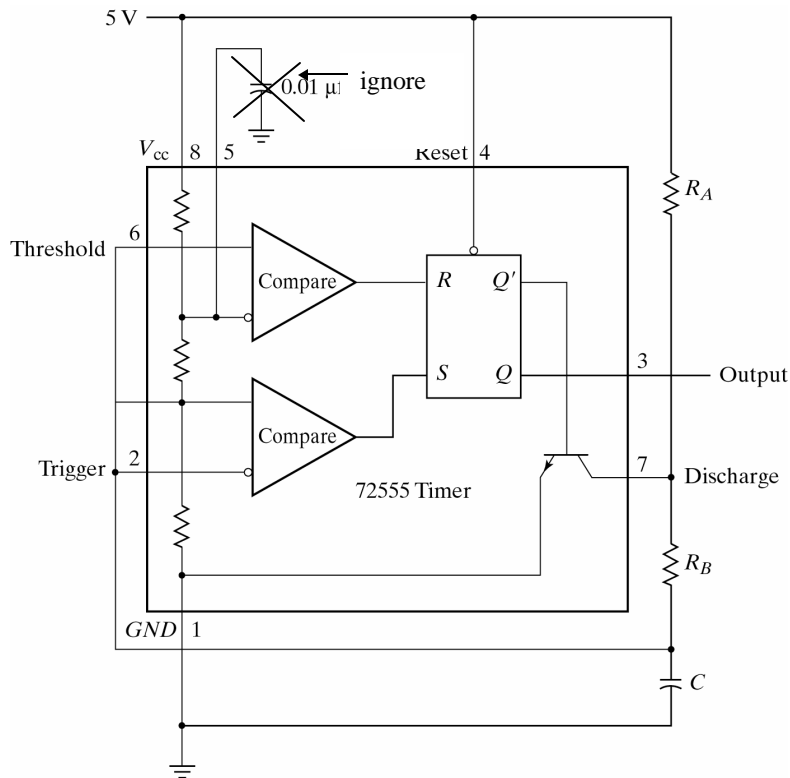


Fig. 11-21 IC Type 72555 Timer Connected as a Clock-Pulse Generator

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