

Registers and Counters

A *register* consists of a group of flip-flops and gates that affect their transition. An n -bit register consists of n -bit flip-flops capable of storing n bits of binary information.

In addition to flip-flops, a register may have combinational gates that perform certain data processing tasks.

A *counter* is essentially a register that goes through a pre-determined sequence of states. The gates in the counter are connected in such a way to produce the prescribed sequence of states.

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BINARY RIPPLE COUNTER

- A binary ripple counter consists of a series connection of complementing flip-flops → the output of each flip-flop is connected to the C input of the next higher-order flip-flop.

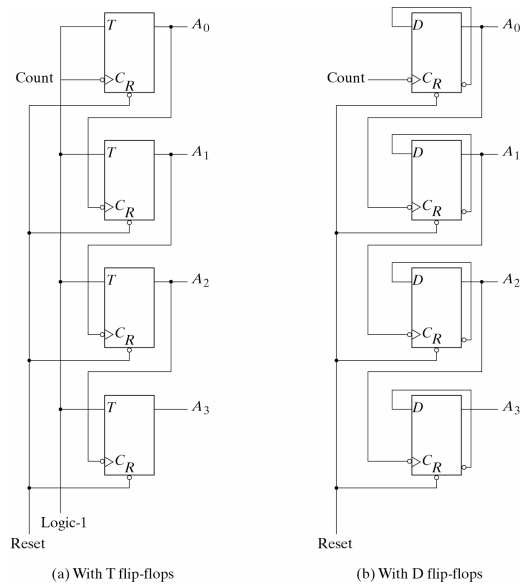


Fig. 6-8 4-Bit Binary Ripple Counter

4-Bit Register

- The common clock input triggers all flip-flops on the positive edge of each pulse → the binary data available at the 4 inputs are transferred into the register.
- The four outputs can be sampled to obtain the binary information stored in the register.
- When the clear input R goes to zero, all flip-flops are reset (register is cleared to 0's).

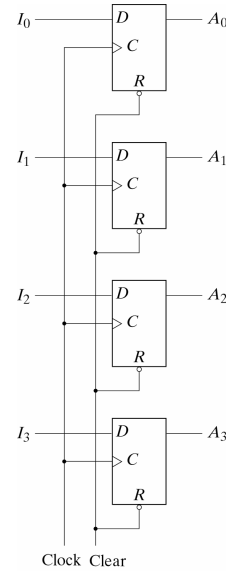


Fig. 6-1 4-Bit Register

Register with Parallel Load

When load input = 1 → data transferred into register with next clock edge.
 When load input = 0 → outputs of Flip-Flops are connected to their inputs.

Q: Why do we want to connect the outputs to the inputs when load input = 0?

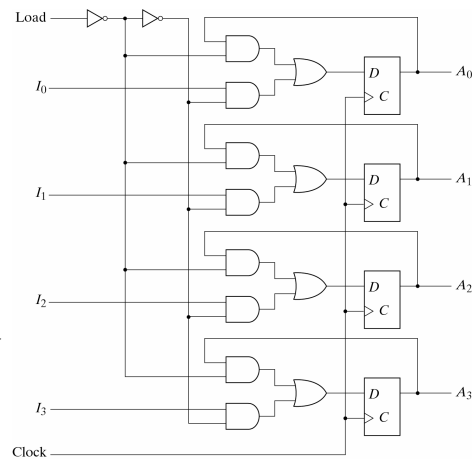


Fig. 6-2 4-Bit Register with Parallel Load

Register with Parallel Load

Example

Design a register with parallel load based on the circuit in Fig 6-2 that operates according to the following function table:

Load	Clear	D	Operation
0	0	A	No change
0	1	0	Clear to 0
1	X	I ₀	Load input

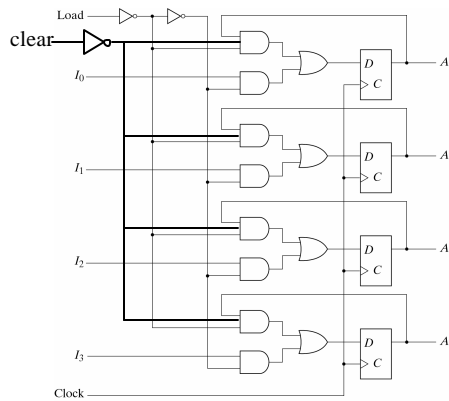
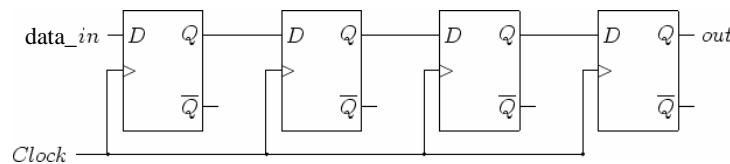


Fig. 6-2 4-Bit Register with Parallel Load

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Shift Registers

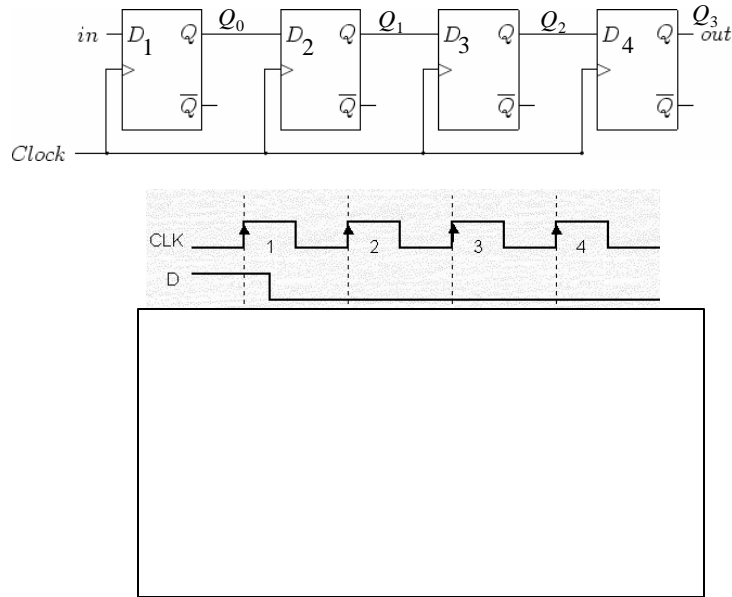
A *Shift Register* is a register that is capable of shifting its binary information in one or both directions.



On the leading edge of the first clock pulse, the signal on the data_in is latched in the first flip-flop. On the leading edge of the next clock pulse, the contents of the first flip-flop is stored in the second flip-flop, and the signal which is present at the data_in is stored in the first flip-flop, *etc.*

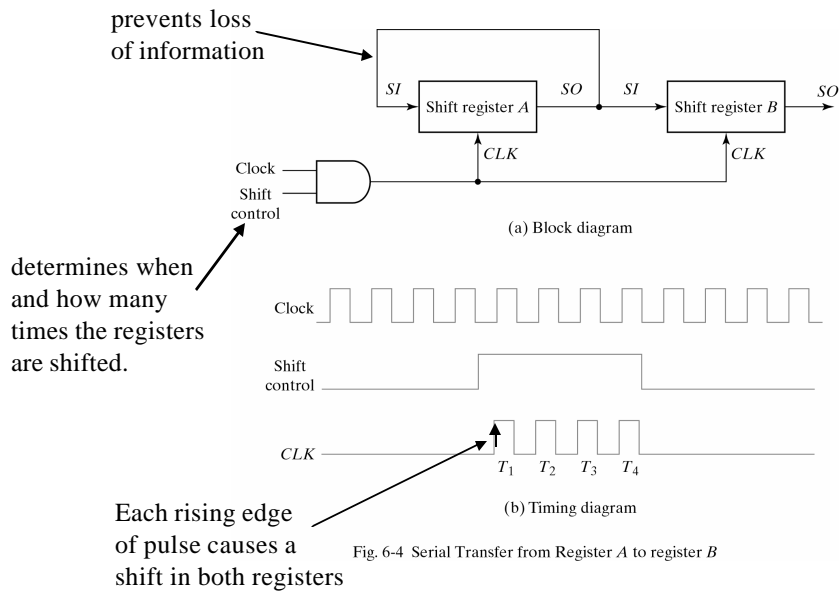
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Serial Shift Registers – Timing Diagram



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Serial Transfer



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Serial Transfer Example 1

	Register A	Register B
Initial Value	1 0 1 1	0 0 1 0
After T_1	?	?
After T_2	?	?
After T_3	?	?
After T_4	?	?

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Serial Transfer Example 1 (contined)

	Register A	Register B
Initial Value		0 0 1 0
After T_1	1 1 0 1	1 0 0 1
After T_2	1 1 1 0	1 1 0 0
After T_3	0 1 1 1	0 1 1 0
After T_4	1 0 1 1	1 0 1 1

With the first pulse T_1 , (a) the rightmost bit of A is shifted into the leftmost bit of B and (b) also circulated into the leftmost position of A . At the same time, (c) all bits of A and B are shifted one position to the right.

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Serial Transfer Example 2

Example 2:

The content of a 4-bit register is initially 1101. The register is shifted 4 times to the right with the serial input being 101101. What is the content of the register after four shifts? Ans: 1101

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Serial/Parallel Computation

Communication between a computer and a peripheral device is usually done serially, while computation in the computer itself is usually performed with parallel logic circuitry.

Computations in the computer are done in parallel because this is a faster mode. Serial operations are slower but require less devices.

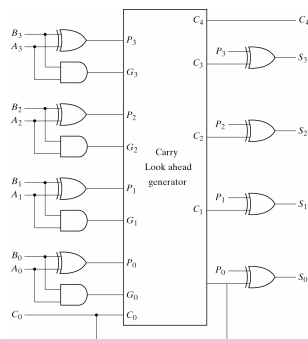


Fig. 4-12 4-Bit Adder with Carry Lookahead

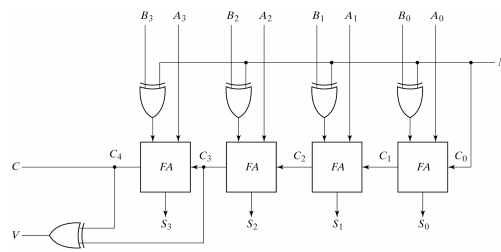
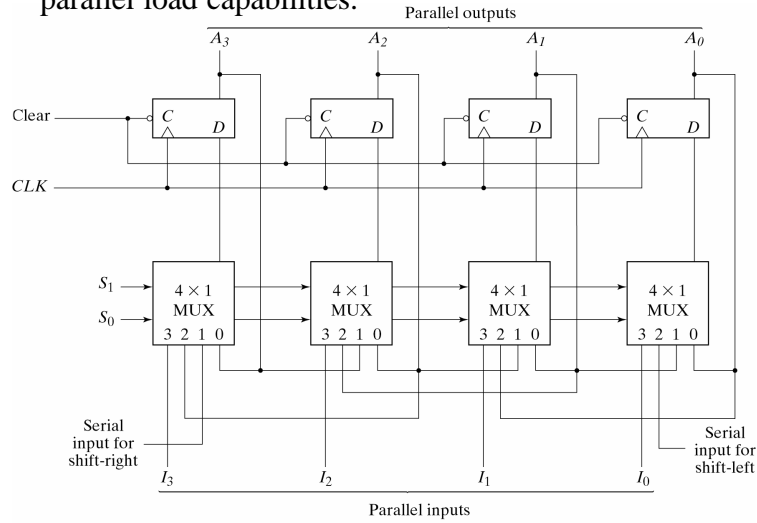


Fig. 4-13 4-Bit Adder Subtractor

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Universal Shift Register

A universal shift register is a bidirectional shift register with parallel load capabilities.



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Fig. 6-7 4-Bit Universal Shift Register

Universal Shift Register

Mode Control		Register Operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

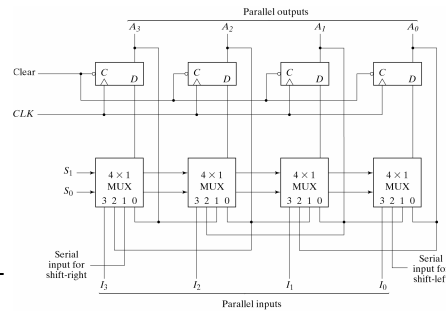


Fig. 6-7 4-Bit Universal Shift Register

- When $S_1 S_0 = 11$, the binary information on the parallel input lines is transferred into the register simultaneously at the next clock edge.
- When $S_1 S_0 = 00$, the present value of the register is applied to the D inputs of the FFs. This forms a conduction path from the output to the input of each FF.
- When $S_1 S_0 = 01$, terminal 1 of the multiplexer inputs has a path to the D inputs of the FFs, which causes a shift-right operation, with serial input transferred into FF A3.
- When $S_1 S_0 = 10$, a shift-left operation results with serial input going into FF A0.

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Parallel vs. Serial Data Transmission

Shift registers are often used to interface digital systems situated remotely from each other.

Task: We want to transmit an n -bit quantity between two location that are far from each other.

What are the options?

1. Use n lines to transmit n bits in parallel. Problem: Cost is expensive.
2. Use a single line to transmit the information serially, one bit at a time. Cost is less.